WE CLAIM:

1. A method of generating a clock signal based on a periodic reference signal, said method comprising:

receiving a periodic reference signal;

generating a clock signal synchronized to said reference signal in response to said receiving;

feeding back said synchronized clock signal;

delaying said fed back synchronized clock signal to maintain synchronization with said reference signal; and

generating a clock signal in response to said delayed fed back signal independent of said reference signal.

2. The method of claim 1 wherein said synchronized clock signal is synchronized to the reference clock signal by phase.

3. The method of claim 1 further comprising multiplexing said periodic reference signal and said delayed fed back signal.

4. The method of claim 1 wherein said synchronized clock signal is generated by a delay-locked loop circuit.

5. The method of claim 1 wherein said synchronized clock signal is generated by a synchronous mirror delay circuit.

6. The method of claim 1 wherein said synchronized clock signal is generated by a measure-controlled delay circuit.

7. The method of claim 1 wherein said generating said synchronized clock signal comprises:

delaying said received periodic reference signal;

measuring the phase difference between said periodic reference signal and said delayed periodic reference signal; and

varying said delaying of said received periodic reference signal to minimize any measured phase difference.

8. The method of claim 1 wherein said generating said synchronized clock signal comprises:

delaying said received periodic reference signal with a first array comprising a series of unit delay elements each having an output;

counting a number of clock cycles;

transferring said delayed periodic signal from one of said delay element outputs of said first array to an input of a second array in response to said counting of clock cycles, said second array comprising a series of unit delay elements each having an input; and

outputting said transferred periodic signal from said second delay array.

9. The method of claim 1 wherein said generating a synchronized clock signal comprises:

inputting said periodic reference signal to a first array and a second array, each of said arrays comprising a series of unit delay elements;

counting a number of clock cycles;

measuring the propagation of said periodic reference signal through said first array in increments of unit delays in response to said number of clock cycles having been counted; and

configuring said second array to output said periodic reference signal upon said measured number of unit delays.

10. A method of generating a clock signal based on a periodic reference signal, said method comprising:

receiving a periodic reference signal;

delaying said periodic reference signal to generate an output clock signal;

feeding back said clock signal;

adjusting said delaying to synchronize said clock signal with said periodic reference signal; and

maintaining said clock signal independent of said reference signal.

11. The method of claim 10 wherein said clock signal is maintained within a delay-locked loop circuit.

12. The method of claim 10 wherein said clock signal is maintained within a synchronous mirror delay circuit.

13. The method of claim 10 wherein said clock signal is maintained within a measure-controlled delay circuit.

14. A method of generating a clock signal based on a periodic reference signal, said method comprising:

delaying said periodic reference signal with a variable delay line;

measuring the phase difference between said periodic reference signal and said delayed periodic reference signal;

varying said delaying of said periodic reference signal based on said measured phase difference to produce a clock signal synchronized to said periodic reference signal;

feeding back said synchronized clock signal to said variable delay line after said measured phase difference is minimized; and

maintaining said synchronization of said fed back clock signal without said periodic reference signal.

15. The method of claim 14 wherein said maintaining further comprises regenerating said fed back signal.

16. The method of claim 15 wherein said regenerating comprises generating a pulse with a predetermined width synchronized to said fed back clock signal.

17. The method of claim 15 wherein said regenerating comprises correcting the duty cycle with a duty cycle correction circuit.

18. A clock synchronization circuit comprising:

a multiplexer having a first input operative to receive a periodic reference signal, a second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a variable delay having an input coupled to said multiplexer output, an output, and a control input, said control input operative to vary the delay of a signal propagating from said variable delay input to said variable delay output;

a delay circuit having an input coupled to said variable delay output and an output coupled to said second input of said multiplexer, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a phase detector having a first input coupled to said multiplexer first input, a second input coupled to said delay circuit output, and an output, said detector operative to detect a phase difference between signals received at its first and second inputs; and

a variable delay control circuit having an input coupled to said phase detector output and an output coupled to said variable delay control input, said variable delay control circuit operative to control the delay of said variable delay.

19. The clock synchronization circuit of claim 18 further comprising:

a buffer circuit having an input and an output, said input operative to receive said periodic reference signal and said output connected to said first input of said multiplexer; and

a second buffer circuit having an input and an output, said input connected to said variable delay line output; wherein:

said delay circuitry has a delay approximately equal to the sum of the delays of said first and second buffer circuits.

20. The clock synchronization circuit of claim 18 further comprising a pulse generator having an input and an output, said pulse generator connected to the output of said variable delay line, wherein said pulse generator is operative to output a pulse of a predetermined width, synchronized with the output of said variable delay line.

21. The clock synchronization circuit of claim 18 further comprising a duty cycle correction circuit having an input and an output, said duty cycle correction circuit input connected to the output of said variable delay line, wherein said duty cycle correction circuit is operative to maintain the duty cycle of said reference signal.

22. A clock synchronization circuit comprising:

a multiplexer having a first input operative to receive a periodic reference signal, a second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a first delay circuit having an input coupled to said multiplexer output and an output, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a first array having an input coupled to said first delay circuit output and a series of delayed periodic signal outputs, each of said outputs providing an output signal with a progressively increasing amount of delay;

a second array having an output and a series inputs, each of said inputs having a progressively increasing amount of delay between it and said second array output;

a counter having an input coupled to receive said periodic reference signal and an output, said counter operative to output a signal after a set number of clock cycles of said periodic reference signal have been counted;

a mirror control circuit having a control input coupled to said counter output, said mirror control circuit operative to transfer said delayed periodic signal from one of said first array outputs to an input of said second array; and

a second delay circuit having an input coupled to said second array output and an output coupled to said multiplexer second input, said delay circuit operative to delay a signal propagating from said second delay circuit input to said second delay circuit output.

23. A clock synchronization circuit comprising:

a first multiplexer having a first input operative to receive a periodic reference signal, a

second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a first delay circuit having an input coupled to said first multiplexer output and an output, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a first array having an input coupled to said first delay circuit output and an output, said first array having a series of delay elements, each of said delay elements providing an output signal with a progressively increasing amount of delay;

a second multiplexer having a first input coupled to said first delay circuit output, a second input coupled to said first multiplexer output, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a counter having an input coupled to said first multiplexer output and an output, said counter operative to output a signal after a set number of clock cycles of a signal received from said first multiplexer output;

a second array having an input coupled to said second multiplexer output and an output, said second array having a series of delay elements, each of said delay elements providing an output signal with a progressively increasing amount of delay; and

a measure circuit having an input coupled to said counter output, said measure circuit operative to measure the number of said first array delay elements said periodic reference signal has propagated through in said set number of clock cycles and further operative to set said second array to propagate a signal through the same number of delay elements.

24. Apparatus for generating a clock signal based on a periodic reference signal, said apparatus comprising:

means for receiving a periodic reference signal;

means for generating a clock signal synchronized to said reference signal in response to said receiving;

means for feeding back said synchronized clock signal;

means for delaying said fed back synchronized clock signal to maintain synchronization with said reference signal; and

means for generating a clock signal in response to said delayed fed back.

25. The apparatus of claim 24 wherein said means for generating said synchronized clock signal comprises:

means for delaying said received periodic reference signal;

means for measuring the phase difference between said periodic reference signal and said delayed periodic reference signal; and

means for varying said means for delaying said received periodic reference signal to minimize said measured phase difference.

26. The apparatus of claim 24 wherein said means for generating said synchronized clock signal comprises:

means for delaying said received periodic reference signal with a first array comprising a series of unit delay elements each having an output;

means for counting a number of clock cycles;

means for transferring said delayed periodic signal from an output of said first array to a second array in response to said counting of clock cycles; and

means for outputting said transferred periodic signal from said second delay array.

27. The apparatus of claim 24 wherein said means for generating a synchronized clock signal comprises:

means for inputting said periodic reference signal to a first array comprising a series of unit delay elements;

means for counting a number of clock cycles;

means for measuring the delay of said delayed periodic reference signal through the first array in increments of unit delays substantially in response to said clock cycles having been counted; and

means for configuring a second array to output said periodic reference signal upon said measured number of unit delays.

28. Apparatus for producing a clock signal based on a periodic reference signal, said apparatus comprising:

means for receiving a periodic reference signal;

means for delaying said periodic reference signal to produce an output clock signal;

means for feeding back said clock signal;

means for adjusting said delaying to synchronize said clock signal with said periodic reference signal; and

means for maintaining said clock signal independent of said reference signal.

29. Apparatus for generating a clock signal based on a periodic reference signal, said apparatus comprising:

means for delaying said periodic reference signal with a variable delay line;

means for measuring the phase difference between said periodic reference signal and said delayed periodic reference signal;

means for varying said delaying of said periodic reference signal based on said measured phase difference to produce a clock signal synchronized to said periodic reference signal;

means for feeding back said synchronized clock signal to said variable delay line after said measured phase difference is minimized; and

means for maintaining the synchronization of said fed back clock signal without said periodic reference signal.

30. The apparatus of claim 29 wherein said means for maintaining further comprises means for regenerating said fed back signal.

31. The apparatus of claim 30 wherein said means for regenerating comprises generating a pulse with a predetermined width synchronized to said fed back signal.

32. The apparatus of claim 30 wherein said means for regenerating comprises means for correcting the duty cycle with a duty cycle correction circuit.

33. A computer system comprising:

a processor;

a memory controller coupled to said processor; and

a plurality of dynamic random access memory (DRAM) chips coupled to said memory controller,

at least one of said DRAM chips comprising a clock synchronization circuit comprising:

a multiplexer having a first input operative to receive a periodic reference signal, a second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a variable delay having an input coupled to said multiplexer output, an output, and a control input, said control input operative to vary the delay of a signal propagating from said variable delay input to said variable delay output;

a delay circuit having an input coupled to said variable delay output and an output coupled to said second input of said multiplexer, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a phase detector having a first input coupled to said multiplexer first input, a second input coupled to said delay circuit output, and an output, said detector operative to detect a phase difference between signals received at its first and second inputs; and

a variable delay control circuit having an input coupled to said phase detector output and an output coupled to said variable delay control input, said variable delay control circuit operative to control the delay of said variable delay.

34. A computer system comprising:

a processor;

a memory controller coupled to said processor; and

a plurality of dynamic random access memory (DRAM) chips coupled to said memory controller, at least one of said DRAM chips comprising a clock synchronization circuit comprising:

a multiplexer having a first input operative to receive a periodic reference signal, a second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a first delay circuit having an input coupled to said multiplexer output and an output, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a first array having an input coupled to said first delay circuit output and a series of delayed periodic signal outputs, each of said outputs providing an output signal with a progressively increasing amount of delay;

a second array having an output and a series inputs, each of said inputs having a progressively increasing amount of delay between it and said second array output;

a counter having an input coupled to receive said periodic reference signal and an output, said counter operative to output a signal after a set number of clock cycles of said periodic reference signal have been counted;

a mirror control circuit having a control input coupled to said counter output, said mirror control circuit operative to transfer said delayed periodic signal from one of said first array outputs to an input of said second array; and

a second delay circuit having an input coupled to said second array output and an output coupled to said multiplexer second input, said delay circuit operative to delay a signal propagating from said second delay circuit input to said second delay circuit output.

35. A computer system comprising:

a processor;

a memory controller coupled to said processor; and

a plurality of dynamic random access memory (DRAM) chips coupled to said memory controller, at least one of said DRAM chips comprising a clock synchronization circuit comprising:

a first multiplexer having a first input operative to receive a periodic reference signal, a second input, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a first delay circuit having an input coupled to said first multiplexer output and an output, said delay circuit operative to delay a signal propagating from said delay circuit input to said delay circuit output;

a first array having an input coupled to said first delay circuit output and an output, said first array having a series of delay elements, each of said delay elements providing an output signal with a progressively increasing amount of delay;

a second multiplexer having a first input coupled to said first delay circuit output, a second input coupled to said first multiplexer output, an output, and a control input operative to select one of said first and second inputs to couple to said output;

a counter having an input coupled to said first multiplexer output and an output, said counter operative to output a signal after a set number of clock cycles of a signal received from said first multiplexer output;

a second array having an input coupled to said second multiplexer output and an output, said second array having a series of delay elements, each of said delay elements providing an output signal with a progressively increasing amount of delay; and

a measure circuit having an input coupled to said counter output, said measure circuit operative to measure the number of said first array delay elements said periodic reference signal has propagated through in said set number of clock cycles and further operative to set said second array to propagate a signal through the same number of delay elements.